REMARKS

Claims 1-20 are pending in the application. Claims 1, 9, and 18 are independent. By the foregoing Amendment, Applicants seek to amend claims 1, 9, and 18. These changes are believed to introduce no new matter and their entry is respectfully requested.

Objection to Claims 1, 9, and 18

In paragraph 3 of the Office Action, the Examiner objected to claims 1, 9, and 18 because of informalities. By the foregoing Amendment, Applicants have amended claims 1, 9, and 18 to accommodate the objection. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the objection.

Rejection of Claims 1-5, 9-13, and 18-20 Under 35 U.S.C. §103(a)

In paragraph 5 of the Office Action, the Examiner rejected claims 1-5, 9-13, and 18-20 under 35 U.S.C. §103(a) as being obvious by U.S. Patent No. 6,356,122 B2 to Sevalia et al. (hereinafter "Sevalia") in view of U.S. Patent No. 5,636,249 to Roither (hereinafter "Roither"). To establish a *prima facie* case of obviousness, an Examiner must show three things: (1) that there is some suggestion or motivation to modify a reference or combine reference teachings to arrive at the claimed invention, (2) that there must be a reasonable expectation of success, and (3) that the references teach or suggest each and every element of the claimed invention (MPEP §2143). Applicants respectfully traverse the rejection.

Independent claims 1 and 9 recites in pertinent part "said second delay element to delay the feedback clock signal, to determine whether a rising edge of the delayed feedback clock signal is early or late with respect to a falling edge of the feedback clock signal, and to increase or decrease the delay of the feedback clock signal based on whether the rising edge of the delayed feedback clock signal is early or late with respect to the falling edge of the feedback clock signal" (emphasis added). Independent claim 18 recites in pertinent part "said delay phase-aligning a falling edge of the feedback clock signal to a rising edge of the delayed feedback clock signal" (emphasis added).

In the Office Action, the Examiner asserts that Sevalia discloses a timing circuit comprising at least one driving circuit (multiplexer) outputting an output signal; a phase locked

loop (conventional PLL) receiving a reference clock signal (ref clock from input pin) and supplying an output clock signal form post divider M) to said at least one driving circuit, the phase locked loop generating said output clock signal according to said received reference clock signal and a delayed feedback clock signal; first and second delay elements (programmable delays DL 1 and DL2) located in the path of the reference clock signal and the path of the feedback clock signal, respectively, said first and second delay elements to delay the feedback clock signal; the delay elements being configured to provide a delay in order to make the output signal meet a predetermined valid data timing requirement and to increase or decrease the delay of the feedback clock signal based on whether an edge of the delayed feedback clock signal is early or late with respect to an edge of the feedback clock signal.

Applicants respectfully disagree with the Examiner's characterization of Sevalia. For example, there is no teaching or suggestion in Sevalia of the delay elements increasing or decreasing the delay of the feedback clock signal based on whether an edge of the delayed feedback clock signal is early or late with respect to an edge of the feedback clock signal. The place in Sevalia that the Examiner relies on to support this proposition, which is column 4, lines 55-58, states "One may alternatively implement the inventive concept (e.g., programmable delay blocks in feedback and/or reference input paths) in a ring oscillator or delay-locked loop circuit." Applicants respectfully submit that this passage does not teach or suggest what the Examiner alleges it does, namely delay elements increasing or decreasing the delay of the feedback clock signal based on whether an edge of the delayed feedback clock signal is early or late with respect to an edge of the feedback clock signal. Accordingly, Applicants respectfully submit that Sevalia is improperly applied to the claimed invention.

In paragraph 8 of the Office Action, the Examiner states that Sevalia does not discuss the details of the delay elements, but in paragraph 9 of the Office Action the Examiner asserts that Roither discloses a timing circuit having delay elements to determine whether a rising edge of the delayed feedback clock signal (rds signal) is early or late with respect to a falling edge of the feedback clock signal (bit rate clock).

Applicants respectfully disagree with the Examiner's characterization of Roither. For example, Applicants respectfully submit that the Examiner's characterization of the RDS signal

as a "delayed feedback clock signal" and the bit rate clock as the "feedback clock signal" is in error. Applicants respectfully submit that the relationship between the RDS signal and the bit rate clock in Roither is not that of the RDS signal being a delayed version of the bit rate clock. For example, Roither teaches at column 1, lines 13-45 that RDS is an abbreviation for Radio Data System, which is a standardized system in Europe for transmitting the name or part of the name of the radio station in a coded manner to radio receivers. On the transmitter side, the RDS signal is modulated onto a 57 KHz carrier, whose frequency is not transmitted to the receiver. Thus, on the receiver end a bit rate clock signal must be produced. This means that the RDS signal is not a delayed version of the bit rate clock as the Examiner asserts, but is created in the transmitter while the bit rate clock is created in the receiver.

Applicants respectfully submit further that the Examiner's assertion that Roither teaches determining whether a rising edge of the delayed feedback clock signal (rds signal) is early or late with respect to a falling edge of the feedback clock signal (bit rate clock) is not actually taught in Roither. The passage cited by the Examiner for the proposition does not teach what the Examiner says it teaches. For example, the passage does not talk about making any type of determination of whether the RDS signal is early or late with respect to the bit rate clock.

In paragraph 10 of the Office Action, the Examiner concludes that it would have been obvious to combine Sevalia with Roither because such combination provides a way to align the edges of signals. Applicants respectfully disagree and submit that the rationale used by the Examiner to combine Sevalia with Roither is an improper rationale. According to MPEP §2143.01, there must be some suggestion or motivation to combine two references, and the combination cannot render a reference unsatisfactory for its intended purpose.

Applicants respectfully submit that the Examiner has failed to make out a *prima facie* case of obviousness of the claims 1, 9, and/or 18 over Sevalia in view of Roither because the combination the Examiner proposes renders Roither unsatisfactory for its intended purpose. For example, Roither is trying make the time it takes for the RDS signal and the bit rate clock to attain phase synchronization as small as possible (i.e., ***speed up phase synchronization*** "bring the bit rate clock signal instantaneously into phase synchronization with the RDS signal"), whereas Sevalia teaches placing programmable delay blocks in the reference clock path or

feedback clock path (i.e., ***delay phase synchronization***). Thus, combining the delay blocks of Sevalia with the timing circuit of Roither would render Roither unsatisfactory for its intended use. Because the Examiner the Examiner has used an improper rationale for combining Sevalia and Roither, the Examiner has failed to make out a *prima facie* case of obviousness of the claims 1, 9, and/or 18 over Sevalia in view of Roither.

Regarding dependent claims 2-5, 10-13, and 19-20, Applicants respectfully submit that the Examiner has failed to make out a *prima facie* case of obviousness over Sevalia in view of Roither as well. Claims 2-5, 10-13, and 19-20 properly depend from independent claims 1, 9, and 18, respectively, and thus incorporate the elements of their respective independent claims. According to MPEP §2143.01, claims 2-5, 10-13, and 19-20 are therefore also not obvious over Sevalia in view of Roither.

Rejection of Claims 6 and 14 Under 35 U.S.C. §103(a)

In paragraph 14 of the Office Action, the Examiner rejected claims 6 and 14 under 35 U.S.C. §103(a) as being unpatentable over Sevalia in view of U.S. Patent No. 5,818,270 to Hamza (hereinafter "Hamza"). Applicants respectfully traverse the rejection.

Applicants respectfully submit that claims 6 and 14 properly depend from patentable claims 1 and 9, respectively, and are therefore patentable as well. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 6 and 14.

Rejection of Claims 7-8 and 15 Under 35 U.S.C. §103(a)

In paragraph 18 of the Office Action, the Examiner rejected claims 7-8 and 15 under 35 U.S.C. §103(a) as being unpatentable over Sevalia as applied to claim 1 and in further view of U.S. Patent No. 5,977,837 to Byrn (hereinafter "Byrn"). Applicants respectfully traverse the rejection.

Applicants respectfully submit that claims 7-8 properly depend from patentable claim 1 and are therefore patentable as well. Applicants respectfully submit that claim 15 properly depends from patentable claim 9 and is therefore patentable as well. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 7-8 and 15.

Rejection of Claims 16-17 Under 35 U.S.C. §103(a)

In paragraph 23 of the Office Action, the Examiner rejected claims 16-17 under 35 U.S.C. §103(a) as being unpatentable over Sevalia as applied to claim 1 and in further view of U.S. Patent No. 5,742,798 to Goldrain (hereinafter "Goldrain"). Applicants respectfully traverse the rejection.

Applicants respectfully submit that claims 16-17 properly depend from patentable claim 9 and are therefore patentable as well. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 16-17.

CONCLUSION

Applicants submit that all grounds for rejection have been properly traversed, accommodated, or rendered moot, and that the application is now in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: March 17, 2005

Jan Little-Washington
Reg. No. 41,181

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